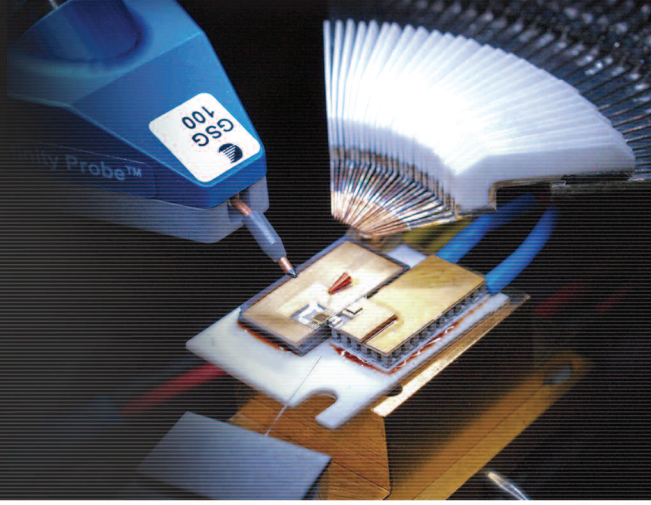

Photonic Integrated Circuits Accessible to Everyone

table of contents

Welcome to the second newsletter of the EU H2020 PICs4All project. Photonic Integrated Circuits (PICs) open up whole new opportunities to create new products and improve existing electronic and photonic devices. The technology of PICs has been subject to research and development in academia and industrial laboratories for several decades and now can be exploited through various open access services, enabling PIC design, manufacturing, testing and packaging. The PICs4All consortium forms a group of experts in the field of photonics, ready to help you and guide through all these services, as well as explain the added value of PICs in your products and applications. Our PIC support centers are distributed around Europe and have experience working with various markets, like high-speed data communication, sensing, biomedical, automotive, where photonic integrated devices can be applied.

In this issue we present use cases of PICs for optical coherence tomography (OCT) and optical gyroscope systems; InP photonic foundry – SMART Photonics shows capabilities of their technology platform; we give an overview of Nazca-Design: an open source photonic IC design framework that can be explotited by photonic designers, foundries and for education purposes; and Photonics Research Labs at Universitat Politecnica de Valencia explain their capabilities for design and extensive testing of PICs, both bare dies and packaged devices.

Katarzyna Ławniczuk (TU/e) and **John Eisses** (Berenschot)

How to contact us:
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Stanisław Stopiński (issue editor): s.stopinski@imio.pw.edu.pl

Generic photonic integration platforms – SMART Photonics

Building on a long-standing reputation for excellence

Headquartered in Eindhoven, The Netherlands, SMART Photonics is a trusted partner of the world's leading companies, large and small, because of its proven track record in InP photonics research, development and production. We have brought together the right expertise in the right place at the right time. Photonic indium phosphide chips are proving to be the best choice in many applications ranging from next generation low-power data-centers to "intelligent pills" for medical diagnostics and high-accuracy drug dispensing. Integrated photonics also plays an increasingly important role in the aircraft industry, air quality monitoring and ultra-secure cryptography.

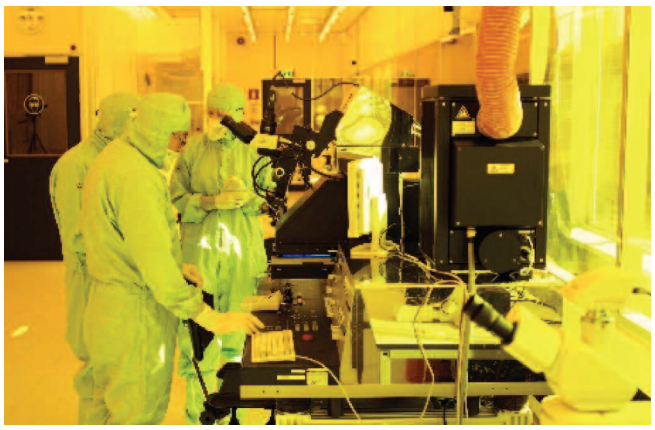
SMART Photonics offers a generic process developed in collaboration with the COBRA research institute, now part of the Institute for Photonic Integration, allowing for fast prototyping and low-cost development without compromising performance and functionality.

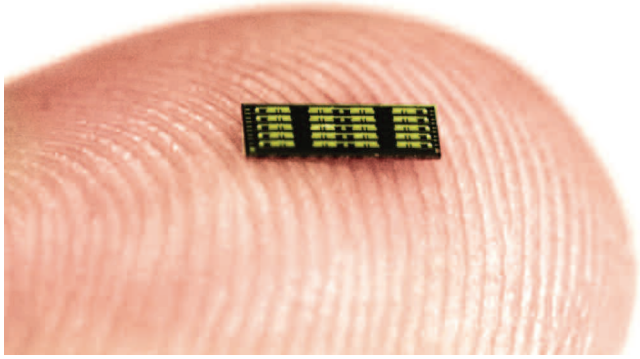
Pure-Play is key to trusted partnerships

SMART Photonics has a deep understanding of the entire process from design to finished production wafers and coated bars of chips. Our approach is in building trusted partnerships with high-tech companies around the world. SMART Photonics is an independent pure-play foundry, we only make products using designs from external customers. The fact that we do not make our own products means there can be no conflict of interest in the market.

The next phase has begun

SMART Photonics was established in March 2012 as the result of a strategic spinout from Eindhoven University of Technology (TU/e) combined with the commercial, industrial and business expertise from former employees of Philips Photonic Labs. Our team (now counting 36 experts) has a broad experience in epitaxial growth and regrowth, processing, ultra-high quality control, and test & measurement.





SMART Photonics expanded its services in September 2015 by opening a second manufacturing facility, located in a purpose-built clean room at the High-Tech Campus Eindhoven. This second cleanroom allowed us to scale-up production. The wafers in our research facility are 2-inch, while the production fab works with 3-inch wafers. To scale the technology even further we are now planning for a new, large scale fab which can handle 4-inch wafers, to be opened in the last quarter of 2018. This will allow further growth of the technology, using a high degree of equipment automation, leading to more stable processing and a reduced cost per chip in high quantities. To make some comparison here on

the generic process, low-volume Multi Project Wafer chips have a price tag of around 80 Euro/mm^2. In volume production, the same chip will cost approximately 10 Euro per mm^2. In the future, it is our ambition to further reduce the cost by an order of magnitude, when high volumes are established for these Photonic IC's. We are not there yet, but it is a very ambitious goal we are trying to achieve with the whole team.

Photonics revolution

If you have any demand or question in the photonics area please start asking around with experts to see if prototyping your idea is possible. A small seed can be enough to grow into the next new innovative product that the world is looking for. The integrated photonics market is growing rapidly and if you are pursuing your idea, you will become a vital part of it. The manufacturing ecosystem for simulations tools and design, chip manufacturing, packaging and testing is in place, allowing everyone to start prototyping at very low investments.

To reduce the cost of prototyping even further, the PhotonDelta cooperative (www.photondelta.eu) hands out "MPW Innovation Grants" with which you can reclaim 50% of the foundry cost, diminishing the hurdle to start exploiting your idea.
If you are new to the photonics community and have no idea where to start, we recommend you to go through Jeppix (www.jeppix.eu). They are a broker for our MPW service and will help you with screening the request and with making all the decisions that need to be made by a designer. Ranging from software choice, design house, chip fabrication, even up to the testing of your device.
If you are more experienced, or have a demand for dedicated wafer runs, please feel free to contact our sales team directly at sales@smartphotonics.nl.

PRODUCTS			
	New	**Extended functionalities** FBG for Medical sensing and positioning 5G Antenna systems LIDAR	**New functionalities create new applications** ?
	Existig	**Same functionality on smaller footprint** Sensing for high tech applications (FBG/Analyzing) Telecom/Datacom	**Same functionality in new applications** Fiber to the chip FBG in aviation/pace Point of care medical anaysis
		Existig	New
		MARKETS	

PICs design and test at Photonics Research Labs (PRL-UPV)

The Photonics Research Labs (PRL) belong to the Institute of Telecommunications and Multimedia Applications (iTEAM) and focus their research activity on different applications of photonics, such as optical analog and digital communications, radio-over-fibre systems, photonic integrated circuits, optical signal processing, sensing and industrial photonics. PRL funds its activity through research projects, R&D contracts and collaboration agreements with the industrial sector. PRL also collaborates actively with VLC Photonics, which is a Spin-Off of the institute, in the area of Photonic Integrated Circuits (PICs).

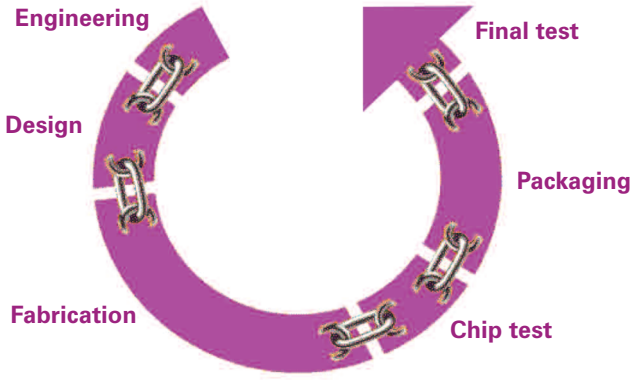
PRL as Application Support Centre (ASC)

PRL has become one of the nine photonics ASCs, experts in photonics, distributed along Europe under the H2020 project PICs4All (Photonic Integrated Circuits for Everyone) which is a Coordination and Support Action whose purpose is to bring closer to researchers and industry the Photonic Integrated Circuits (PICs) technology. In particular, PICs4All aims at assisting on getting access to advanced fabrication facilities for PICs, and enhancing cooperation between research centres, technology clusters and industry, as mentioned in the previous newsletter.

Designing and characterising along the PIC development cycle

The whole development cycle can take up to one year depending on the complexity of the design and the chosen technology platform or foundry. In the following, we highlight the importance of the design and characterization phases since they are considered bottlenecks if your organization does not have the capabilities in terms of experience, tools and equipment.

The **design process** is critical since all the decisions at this early stage will have impact several months later, which represent up to 8 months of your developments and 90% of your investment. The design must consider the fabrication technology platform and must also satisfy several rules for the layout of the design imposed by the foundry. At this stage, you will also need to take into account some packaging and thermal considerations, just to foresee future packaging of your chips. In addition to the experience in design, you will need several dedicated software tools to perform simulations at device, circuit or system levels, depending on your application. Moreover you will need software tools to create the mask layout and to verify it before the submission to the foundry.

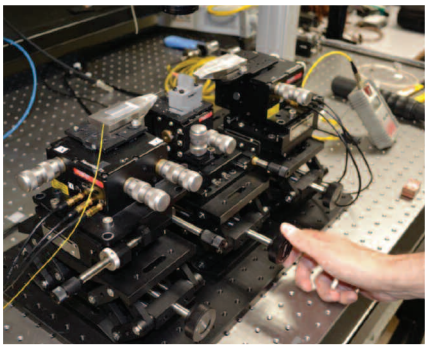
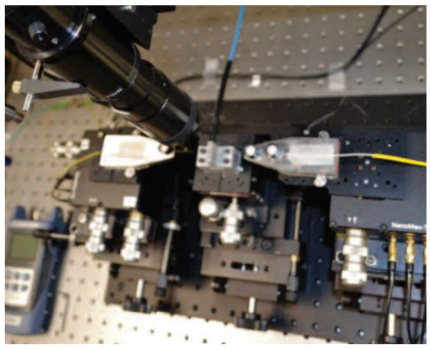
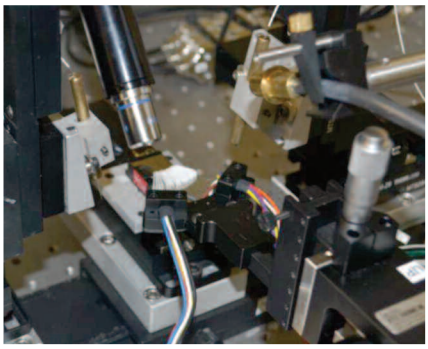


Once fabricated the PIC, its **characterization** may be performed before packaging in order to check the target performance, and also after packaging to check if this process has modified the overall PIC response. In the following, we briefly describe the PIC characterization setups in our labs:

- **Fibres and objectives.** Since the bare PIC has to be accessed from the outside world you will need objectives or optical fibres to coupling in/out the light, which can be standard for vertical coupling, using fibre grating couplers, or lensed fibres for lateral coupling.

- **Chip holders and temperature controllers.** A vacuum holder fixes the chip, avoiding its movement once aligned the PIC coupling structures and the fibres/objectives. Since the PIC's response is temperature dependent, it is thermally controlled through the holder using a temperature controller system.
- **Micro-positioners and motion controllers.** The alignment process between the optical fibres /objectives and the I/O coupling structures of your PIC is performed by a set of piezo positioner stages. As an initial approach to the desired location, the positioners have a manual fine resolution in the order of tens of microns while the final approach is performed using the piezos which are externally controlled, providing a positioning resolution in the order of several nanometres.
- **RF and DC probes.** PICs integrating active elements will need to use, depending on the application, special RF and DC probes mounted on different XYZ stages in order to take the probes to the contact pads in your circuit.
- A **vision system** will also be essential to observe the previous alignment processes along the chip. This system consists basically on a high-magnification zoom lens attached to a high resolution CCD camera which is connected to monitor display. Since the field of view is very small you will need to mount the vision system on a XYZ motorized system to look over the entire chip.

In addition to the mentioned setup to access the PIC, optical and electrical equipment (depending on the application) is required to generate and analyse signals in order to characterize the PIC. At the end, a PIC characterization setup, including equipment, costs several hundred thousand euros, and considering also the costs for the design software licenses, it makes some emerging companies deciding to subcontract such tasks. **At PRL we have fully equipped laboratories in photonics including four full semi-automated PIC characterization setups with dedicated labour force (PIC lab technicians) to assist you**, as well as commercial and proprietary PIC design software, which combined with the extensive equipment list, makes PRL being a privileged setting where to deal cutting-edge technological solutions in PICs.

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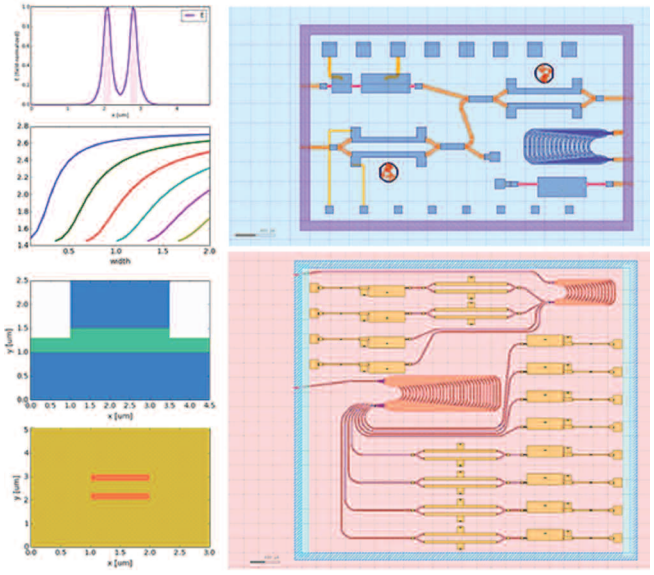
You can also follow us at @upvpiclabs

Nazca Design
Open Source PIC Design Framework

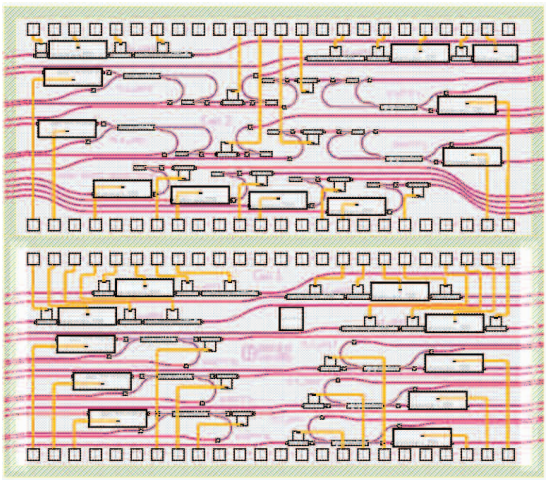
We imagined the PIC design tool that would best support our commercial and research activities. With a team of professional photonic designers we created Nazca. This article explains what Nazca is and how you get started.

Nazca Design [1] is an open source photonic IC design framework for designers, by designers. It is written in Python [2]. Nazca aims to make designers' lives easier when creating either simple or very complex mask designs for MPW or custom PIC platforms. Nazca offers a complete and feature rich framework, including PDK support, mode solvers and waveguide cross section analysis. MPW & packaging templates and fast & flexible mask assembly.



An impression of Nazca Design showing features such as mask layout, waveguide definition and mode-solving

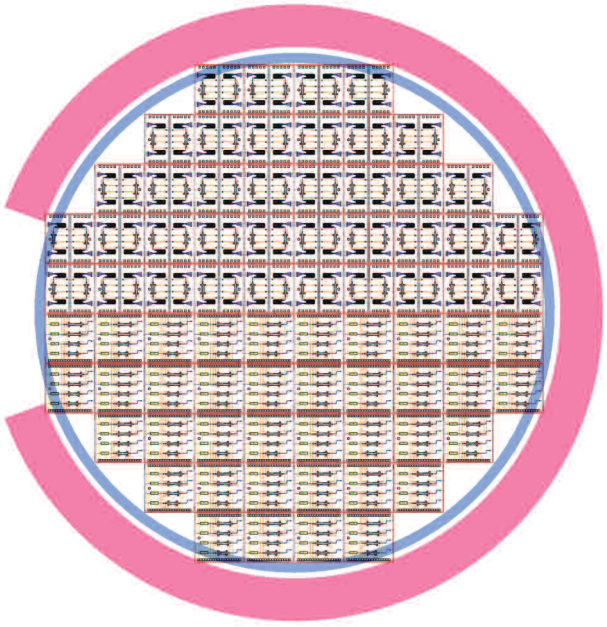
Nazca is based on best practice of experienced PIC designers and rethinks the design flow from the ground up. An important consideration is that PIC mask layout design largely is, and will remain, scripting based. Python is an excellent choice as engineering and scientific scripting language. It is mature, favors simple over complex, and considers code readability as very important. Python allows us to fully embrace the latest software developments such as Jupyter notebooks [3] which are already famous for scientific computing, plotting and creating interactive documents and now also allow for interactive and inline mask design. Python comes with a ton of scientific, mathematical and visualization libraries and is overall the most popular language at the moment with a very fast learning curve. No wonder it effectively is becoming the standard scripting language in photonic design.



Example of a design created with Nazca by Bright Photonics [4] on a Smart Photonics multi project wafer (MPW). It shows how a single 4 x 4 mm^2 MPW cell has been divided into two mini projects via packaging templates. The ease of this kind of hierarchical and flexible design is a key feature of Nazca

Nazca covers PIC design in InP, Silicon Photonics, SiN, polymers, glass and other technologies.
It has been employed in designs at wavelengths ranging from 200 to 2000 nm, in commercial projects as well as in EU research projects like Phoxtrot [5] and L3Matrix [6]. Nazca works smoothly with the open source Klayout mask viewer/editor [7], delivering high-level design via drag & drop. At low level, the Nazca netlist implementation underpins PIC design through intuitive connectivity concepts, which

seek to automate layout options rather than bugging the designer with the obvious. Nazca's goal, beside easy of use, is to maximize design quality at the GDS level, which is critical as the GDS file is the currency between the designer and the foundry.



Nazca mask assembly example for a 3" wafer for the Fraunhofer HHI platform. Generating the mask file from the individual cells/projects takes a few seconds

the Nazca Design Team:

[1] **Nazca**, http://nazca-design.org/
[2] **Python**, https://www.python.org/
[3] **Jupyter**, http://jupyter.org/
[4] **Bright Photonics B.V.**, http://brightphotonics.eu/
[5] **FP7 Phoxtrot project**, http://www.phoxtrot.eu/
[6] **H2020 L3Matrix project**, http://l3matrix.eu/
[7] **Klayout**, http://klayout.de/

Nazca design
photonic IC design framework

For who is Nazca?

1. Designers

Any designer creating a PIC design in a cell or a full mask on an MPW or custom platform.

2. Foundries

Nazca lowers access barriers to a foundry for PIC designers. It provides an easy way to create, distribute and maintain process design kits (PDK). It also provides a secure path for dealing with IP-block libraries from foundries, commercial designers and/or universities. Nazca includes fast and flexible mask assembly with parametrized building blocks and IP-block replacement.

3. Education

Nazca is open source and free. Via Python standards it provides server based and/or quick install access on Windows, Linux, Mac for group training or self education. Nazca stimulates multi-user design and code sharing. The interactive interface allows for a playful exposure of students to PIC design. It visualizes design progress step by step. Also, it offers on demand access to building block and foundry information, such as library content and layer info.

It is fair to say that Nazca guarantees maximum customizability. It avoids code lock-in, stimulates code reuse and sharing, and accelerates open innovation. We believe Nazca has what you need for your next PIC project. Download it at nazca-design.org.

ASPICs for optical gyroscope systems

Modern inertial measurement units (IMUs) require accurate and reliable sensors of the angular velocity. Contemporary optical gyroscopes, characterized by excellent performance combined with low-weight and low energy consumption, are nowadays typically constructed from discrete optoelectronic components. Since 2013 the Institute of Microelectronics and Optoelectronics (IMiO) of Warsaw University of Technology investigates possibility of implementing application specific photonic integrated circuits (ASPICs) in new generation of optical gyroscope systems. Such a solution could provide even further reduction of weight and energy consumption, while simultaneously maintaining high performance of the device.

IMiO has been investigating two different types of optical gyros, both equipped with ASPIC realized in generic integration technology based on indium phosphide platform. The first is the interferometric fiber-optic gyroscope (IFOG), in which the rotation rate is measured by monitoring an interference signal using an ASPIC-based interrogator (**Figure 1** presents a microscope picture of the fabricated device).
The second approach is a fully integrated optical gyro, which can be realized by implementation of a single-frequency ring laser together with a read-out circuit for beating signal detection (**Figure 2** presents a photograph of such an integrated device). First characterization results are promising with respect to implementation of ASPICs in optical gyroscope systems.

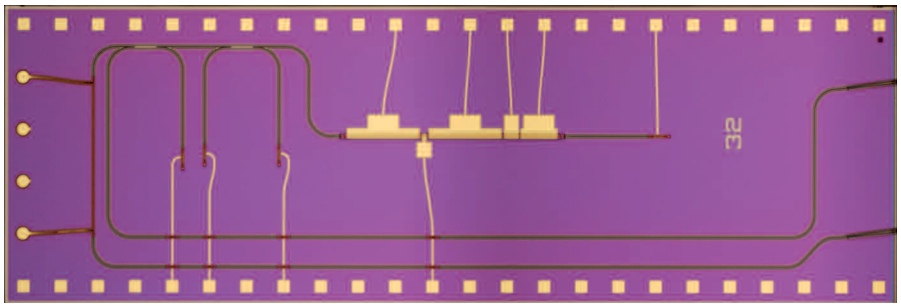


Figure 1. Microscope photograph of the ASPIC interrogator for the interferometric fiber-optic gyroscope system.

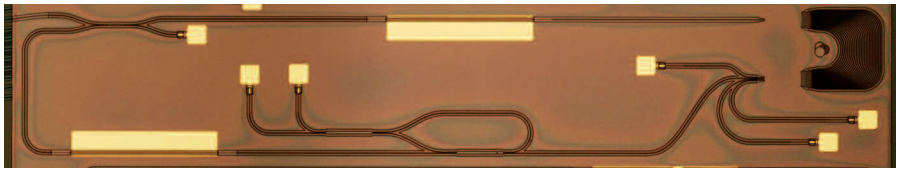


Figure 2. Microscope photograph of the fully integrated optical gyroscope based on a single-frequency ring laser.

IMiO

For more information please contact:

S.Stopinski@imio.pw.edu.pl, the technical manager of the Eastern Europe Design Hub at IMiO.

ASPICs for optical coherence tomography systems

Optical coherence tomography (OCT) has gained a lot of relevance among contact-free imaging techniques. Its classical counterpart, ultrasound, uses acoustic waves and is therefore intrinsically inferior in terms of spatial resolution. Since OCT uses coherent light, it can resolve in the micron range even in strongly scattering materials. This has led to not only a scientific interest in the method, but also a substantial CAGR of the market.

Given the number of optical components required for an OCT system, implementation in an integrated chip seems promising to lower cost and stability.

A key challenge so far was polarization control, since the back-scattered signal is of arbitrary polarization and integrated spectrometers are typically highly polarization sensitive. But since FhG-HHI offers polarization elements in its integration platform, they went ahead together with Berlin-based Verolum GmbH to start the IBB-funded project HIPPIOS. The scope of this project is the development of integrated chip-based OCT systems all the way until market ready prototypes.

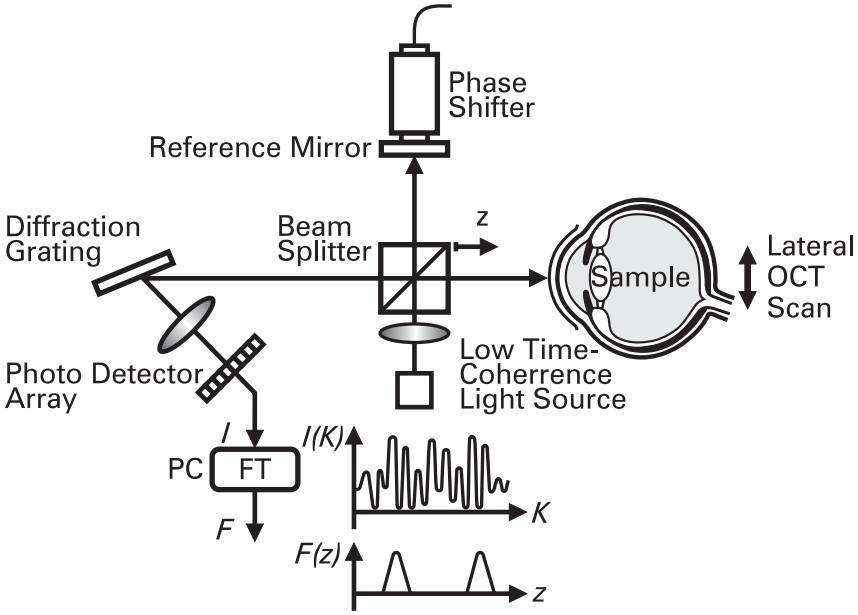
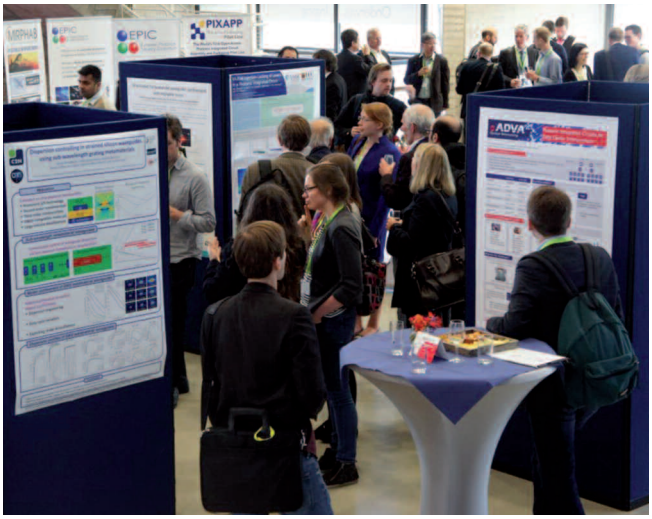


Figure 1, Operation principle of spectrometer-based OCT

Events

The European Conference on Integrated Optics (ECIO 2017)

The European Conference on Integrated Optics (ECIO 2017, https://www.ecio-conference.org/) was held in the "Lichtstad" (City of Light) Eindhoven, The Netherlands, on April 3–5. It attracted almost 200 people, with another 50 attendants for the co-located workshop OWTNM on numerical waveguide modeling. The attendees could enjoy over 70 oral presentations and more than 40 posters, on all aspects of photonic integration and integrated optics. There were many highlights, both from seasoned researchers and from new talents. In this latter category definitely the winners of the presentation and the poster prizes should be mentioned: **Youwen Fan** from the University of Twente impressed with a Optically integrated InP-Si3N4 hybrid laser, while **Daniel Grajales**, from CSIC / ICN2, caught the attention with results on a Bimodal Waveguide Interferometer Biosensor.



The poster session at the ECIO 2017 was a perfect mixture of scientific and social interactions

EUROPEAN CONFERENCE ON INTEGRATED OPTICS

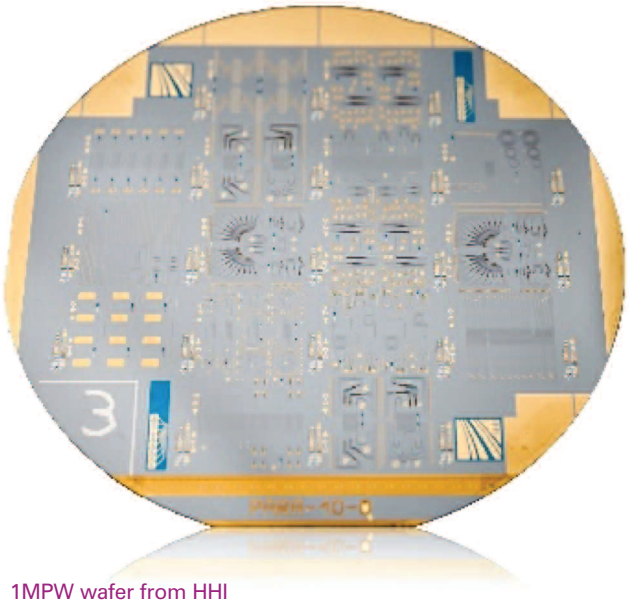
Apart from these technical and scientific presentations, the conference also included a well-attended exhibition, which provided useful interactions for the integrated optics community with a range of companies. A special session was finally dedicated to the emerging Open Access Technologies. You can read more about that in the separate frame.

The next ECIO will be held in Valencia, Spain, in the spring of 2018. Don't miss this exciting event! See you there.

Jos van der Tol

Workshop:
PIC open access platforms

The workshop presented at ECIO 2017 in Eindhoven aimed to inform and engage non expert or first time audience into Photonic Integration Technology using open access platforms. In this special edition experts from InP, Si and SiN materials presented the possibilities of designing photonic chips using generic open access platforms via Multi Project Wafer Runs. Along the workshop we learned that generic integration can be of great help for non-experts designers and PICs prototyping. The process to submit a design to an MPW run was explained giving clear examples fabricated in the different platforms for a broad number of application fields. Including but not limited to communications, terahertz technology, automotive, bio medical etc.



1MPW wafer from HHI

We are very happy to the response of the audience and the further interest on these technologies. Our mission is clear: let the world know that photonics exists and it can be helpful for their on purposes and when it comes to PICs imagination is the limit.

Aura Higuera Rodriguez

GENERIC INTEGRATION
TECHNOLOGIES FOR PHOTONICS

IMiO

JUNE 2018

WARSAW UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRONICS AND INFORMATION TECHNOLOGY

About PICs4All

PICs4All (Photonic Integrated Circuits Accessible to Everyone) is a Coordination and Support Action from the EU H2020 ICT-27-2015 programme. The prime objective of PICs4All is to increase the impact of photonics and enable an access to the advanced photonic integrated circuit (PIC) technologies for academia, research institutes, SMEs and larger companies. This will be achieved by establishing a European network of Application Support Centres (ASCs) in the field of PIC technology. The main task of the ASCs is to lower the barrier to researchers and SMEs for applying advanced PICs, and thus to increase the awareness of the existence of the worldwide unique facility provided by JePPIX (InP and TriPleX PIC design, manufacturing, testing and packaging).

The main PICs4All objectives:

- scouting, acquiring and supporting new PIC users;
- promoting the use of the European photonic integration platforms;
- strengthening Europe's industrial lead in the business of integrated photonics;
- bringing together academia to explore photonics and promote its critical importance.

The PICs4All consortium:

- actively explores the market, searching for new application fields for ASPICs;
- offers guided access to Multi-Project Wafer runs for ASPIC fabrication;
- provides support in ASPIC design and prototype testing;
- connects users to professional design houses and packaging vendors;
- organizes ASPIC design courses and workshops.

PICs4All ASCs will actively support users in taking full advantage of the PIC-technology and its deployment in existing and new applications. For this reason, it combines two targets of an EC supported CSA, i.e. enabling the access to advanced design, fabrication and characterisation facilities, and stimulating the innovation potential of users, esp. SMEs, by supplying hands-on support in developing their business cases. All this is achieved by connecting existing PIC-development infrastructure throughout Europe and by lowering the risk at the investment stage in PIC development by enabling access to low-cost prototyping.

Fact and Figures:

Project reference:	EU H2020-ICT-27-2015 CSA no 687777
Project acronym:	PICs4All (Photonic Integrated Circuits Accessible to Everyone)
Timeline:	1 January 2016–31 December 2018
Budget:	1 051 895,- EUR
Website:	http://pics4all.jeppix.eu
E-mail:	pics4all@jeppix.eu
Coordinator:	Katarzyna Ławniczuk (TU/e) k.lawniczuk@tue.nl

Partners:

The PICs4All consortium consists of nine academic research institutes with a good regional balance throughout Europe, enabling Application Support Centres in Germany, United Kingdom, France, Denmark, Spain, Poland, Italy, Greece, the Netherlands. It also includes the EPIC association located in France and Berenschot in the Netherlands.

Members of the consortium:

Eindhoven University of Technology
University of Cambridge
Universitat Politècnica de València
Politecnico di Milano
Warsaw University of Technology
Technische Universität Berlin
Aarhus University
Telecom ParisTech
National Technical University of Athens
European Photonics Industry Consortium
Berenschot

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dtp: Hanna Sater