

Photonic Integrated Circuits Accessible to Everyone

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Welcome to this April edition of the newsletter of the H2020 PICs4All project. 2019 marks a new phase in photonic integration foundry technology with the launch of the new EC Manufacturing Pilot Line for indium phosphide photonic integrated circuits. InPulse enables businesses to transition seamlessly from their first prototypes to pilot production and beyond. The consortium of foundries, design tool, test tool developers and PIC experts will focus on stabilizing highly interlinked design flows, manufacturing processes and automated testing methods to remove bottlenecks, accelerate time to market, and reduce the barriers for new entrant businesses. Find out more at inpulse.jeppix.eu.

This is the fourth of the Manufacturing Pilot Lines focusing on photonic integrated circuits. PIX4LIFE.eu already offers silicon nitride circuits for visible light circuits widely used in the bio-sciences. PIXAPPeu provides access to packaging technologies and a route to pilot manufacturing. Another recent addition is OIP4NWE.eu which focusses on a new generation of fabrication equipment to ensure that the next PIC technology nodes

enable higher yields, higher precision and a richer design space. An ambition for the pilot lines is to ensure a resilient and sustainable model for long-term access to state of the art manufacturing to a wide range of innovators and entrepreneurs. PICs4All Application Support Centers are on hand to provide orientation and expert advice.

In this issue we present the PICs4All application support center at Politecnico di Milano in Italy. Application notes are highlighted for the topics of delay lines which may play an important role in microwave signal processing, and also quantum technologies which exploit the rich properties of single photons which are controlled and exploitable within integrated circuits. In this issue we also highlight the methods for accessing packaging solutions, both in terms of off-the-shelf solutions using reference designs, and also in terms of the techniques and technologies to ramp to Pilot Production and beyond. As ever, we encourage you to reach out to your local PICs4All application support center to find out how you can take the next steps towards your own PIC-enabled solutions.

Kevin Williams (TU/e)

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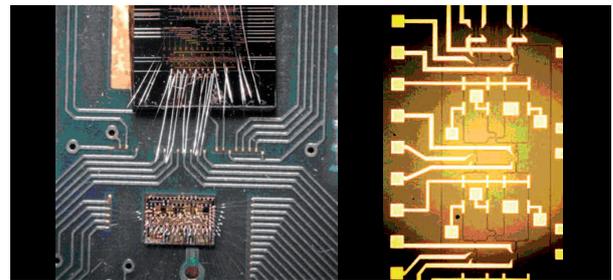
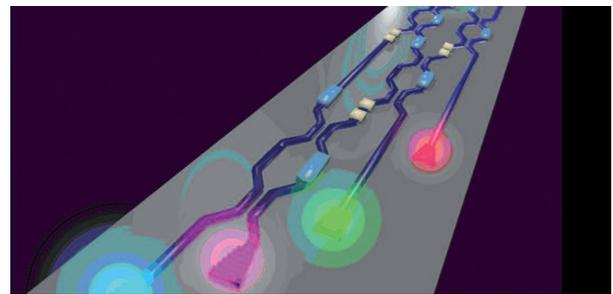
Application Support Center @ Politecnico di Milano, Italy

In Italy the Application Support Center is located in Politecnico di Milano, Dipartimento di Elettronica, Informazione e Bioingegneria. Under the direction of Proff. Andrea Melloni and Francesco Morichetti, the *Photonic Devices Lab* gathers the experience of 25 years of fundamental and applied research in the field of integrated optical technologies on modelling, design and characterization of devices in any technological platform.

The Photonic Devices Group owns laboratories equipped with five optical benches suitable for a broad range of measurement and testing from single waveguides to complex photonic circuits up to 100 Gbaud/s at telecom wavelengths.

The research focuses on passive and controllable devices for high bit rates optical communication systems and optical interconnects, optical signal processing and sensors, materials for integrated photonics, smart actuators, transparent detectors and state of the art on PICs control techniques. The ASC at PoliMi has a wide portfolio of expertise

and tools and is a reference pivot for regional industries and several research groups in Italy and beyond for waveguiding, PICs and multiphysics analysis and design, PICs control strategies with dedicated electronic boards and ASICS.



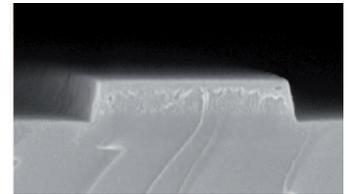
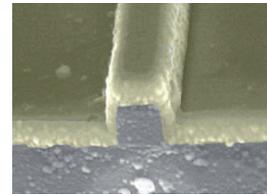
The Photonic Device Group have access to the open access **Polifab** facility, the micro and nano technology center of the Politecnico di Milano created to provide the highest technological standards for a wide range of applications and processes involving others Key Enabling Technologies: photonics, micro and nanoelectronics, biotechnologies, advanced materials and nanotechnology.



Polifab is an open-access, pay-per-use facility, open to research groups of Politecnico as well as to external research institutions and industries. Researchers can work in the cleanroom with the support of the technical staff. Processes can be run directly by the users and by the technical staff of Polifab and offered as a service to external companies or research groups.



Polifab 370 m² clean room provides a flexible support for proof-of-concepts on materials, processes and devices, as well as a fast prototyping of innovative devices in the fields of photonics, microfluidics, lab-on-chip, micromechanics, spintronics, magneto devices, organic electronics, etc. The cleanroom is equipped with advanced instrumentation for the research and development of new materials, technological processes and devices at the micro- and nano-scale.



POLITECNICO
MILANO 1863



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Among the many support activities carried on during PICs4All projects it's worth to mention two successful stories leading to the startup PhotonPath and an industrial project with Optical Sensing Technology.

Reconfigurable Photonic Integrated Circuits for High Capacity Optical Networks

PhotonPath, a just born startup from a PhD of the Photonic Device Group of PoliMI, tackles the issues of traffic saturation and failure of optical networks with grounds in two main foundations: Integrated Photonic Circuits and distinguished support of network reconfigurability. The advantages of PICs include the simplification of assembly processes, reduction of power consumption and footprint. On the other hand, the network reconfigurability is a key feature in a saturated and power-hungry network operating scenario. Either to act in the case of equipment failures and fiber cuts, or to support different traffic requirements and expand network capacity. To fulfill such demand the network elements must be flexible, compact and deliver high performance. Today, the components providing needed optical networks reconfigurability features are bulky, costly and consume lots of power.

PhotonPath benefited of the guidance and assistance of PoliMI ASC and conceived solutions providing reconfigurable PICs that make this flexibility possible, in a scalable and power efficient way. The proof of concept device is being fabricated at Polifab, the micro and nano technology center of Politecnico di Milano. PhotonPath gained notice in three startup competitions held in Italy, arriving at second place at Start-Cup Lombardia in 2018, being among winners of Switch2Product competition from Politecnico di Milano, and as finalist of the Premio Nazionale di Innovazione in 2018.



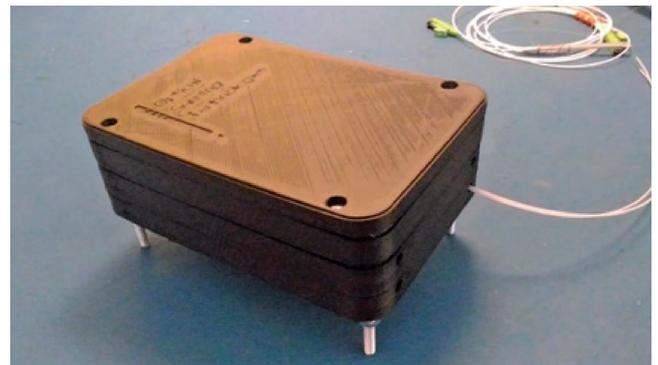
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PICs for sensor interrogators

OST is a Small Enterprise operating in the field of fiber optic sensing, focused on the development of custom interrogation devices to fulfill the requirements of specific industrial exigencies.

Recently, the close collaboration with Politecnico di Milano through its ASC strengthened the role of OST as a bridge between university and industry, allowing to identify the company as a bearer of innovation and launching a project for sensing applications based on Silicon Photonics.



Although fiber optic sensors are widely used in structural monitoring applications, the decoupling of thermal effects from mechanical effects in embedded optical fibers is still an issue. OST developed an innovative Fiber Bragg Grating (FBG) sensors inscribed into a Polarization Maintaining (PM) fiber:

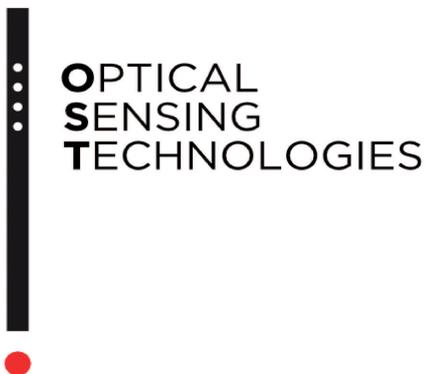


the difference in refractive index of fast and slow fiber axes generates two spectral reflection peaks produced by the FBG, providing two measurements detecting both strain and temperature with a single sensor.

With the guidance of PoliMI ASC, OST conceived a very compact interrogation unit to be embedded into the product of the Customer suitable for in-field operation. The interrogator unit is capable of handling signals generated by the PM fiber, it is miniaturized, simple, fast, accurate, affordable and cost effective to meet industrial requirements.

The solution, based on a Silicon Photonics Micro-Ring Resonator used as a wavelength scanner to detect the dual-peak spectral response of a chain of PM-FBG sensors, is now in the testing phase.

While OST is focused on the system-level design, the design, simulation, packaging and characterization of the Silicon Photonics device is carried on with the support of prof. Andrea Melloni and his team.



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Photonic Integrated Circuits for Tunable Delay Lines

A delay line is a device that allows inducing the propagation delay of signals, ensuring a true-time-delay operation.

In general, inducing a temporal delay on a signal over a large operative bandwidth is not an easy task. Apart digital electronics that can take advantage of shift registers for a discrete arbitrary delay, in analog electronics, microwave and photonics a continuously variable delay without moving parts is difficult to achieve. However, integrated photonic circuits offer a number of solutions to achieve true-time-delay in very compact, flexible and potentially low-cost devices.

A typical application of a delay line is shown in **Fig. 1** where an absolute delay on an optical signal or a relative delay between two signals for synchronization purposes is achieved. The delay Δt should be continuously controllable, induce negligible attenuation and have sufficient bandwidth to let the pulses go through undistorted.

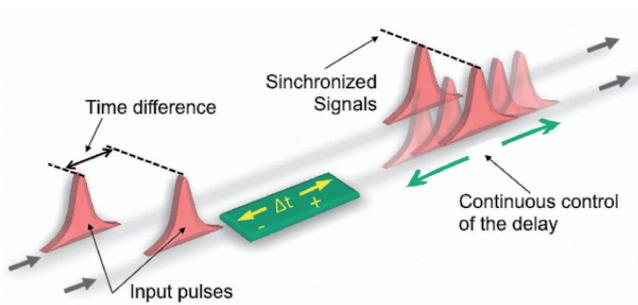


Figure 1 Typical use of a delay line: synchronization of two signals

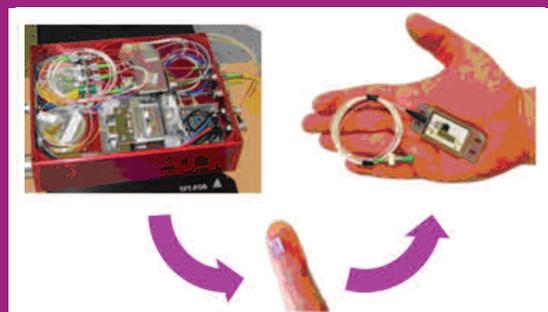
There are a large number of applications where delay lines play a key role: optical beam forming networks for antenna arrays, imaging processing units, radio-on-fiber links and devices, interferometry, sensing units, etc. In case the signal is elec-

Photonic Integrated Circuits (PICs)

Also known as optical chips, PICs can contain tens to hundreds of optical components. While electronic ICs consist of transistors, capacitors and resistors, a PIC consists of, for example, lasers, modulators, photodetectors and filters, all integrated on a single substrate. These PICs are nowadays extensively used commercially, mainly in datacom and telecom.

PIC technology has now become accessible to users without a cleanroom, through so-called multi-project wafer runs and open foundries. Indium phosphide based technology is commercially available through SMART Photonics and Heinrich Hertz Institute. Access is coordinated by the JePIX platform:

<http://www.jepix.eu/>.



trical, it could be convenient to modulate the light generated by a laser with the RF signal, delay in the optical domain and convert back to electrical by means of a photodiode.

Using a proper technology (indium phosphide), the laser, modulator and photodiode can be integrated on the same photonic integrated circuit (PIC), providing a very compact, electrically terminated, robust device. This is a classical expedient that goes under the generic name of microwave photonics.

Photonic Delay Lines

Fig. 2 shows three examples of photonics delay lines integrated on chip. The spiral **a)** induces a fixed delay and it is the integrated version of the classical coils of optical fibers or coaxial cables used in many bulk applications. This is the basic element to realize, in combination with integrated 2×2 switches, delay lines providing a discrete number of fixed delays. It has a very small footprint, low losses, huge bandwidth and does not require any external control. **Fig. 2** shows in **b)** a coupled Ring Resonators based delay line and in **c)** a Mach-Zehnder based single stage delay line. Both solutions provide a continuously tunable delay and can be electrically controllable thanks to proper thermal controllers placed above the waveguides.

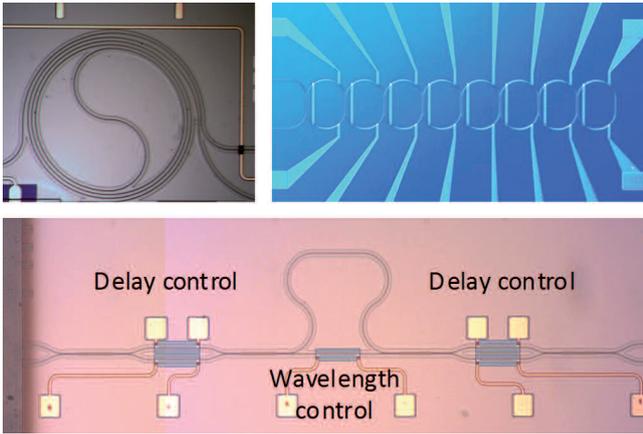


Figure 2 *a)* Fixed delay line; *b)* Coupled Ring Resonator based tunable delay line; *c)* Mach-Zehnder based single stage continuously tunable delay line

Devices inducing a variable time delay up to few nanoseconds have been realized and successfully tested. These devices require a suitable electronic and software to achieve the control and stabilization against thermal and other fluctuations and be adaptive to the variations of the input signals.

Potentials and Limits

The ring-based delay line is a popular solution because of the very small footprint. Tunability is

achieved by changing the resonant frequency, and the combination of various rings provides shaping of the spectral region in which the delay is achieved. The bandwidth, instead, is usually narrow and the achieved bandwidth-delay product is rather small.

The Mach-Zehnder based delay line has a much larger bandwidth-delay product and induces a very small distortion on the delayed signals. Several stages can be cascaded to achieve a longer delay, still maintaining a large bandwidth as shown in **Fig. 3** for a double stage device. Only one electrical control is required to change the coupling coefficient K of the directional couplers. Further, being a 2×2 circuit, it can provide a differential delay between two input signals.

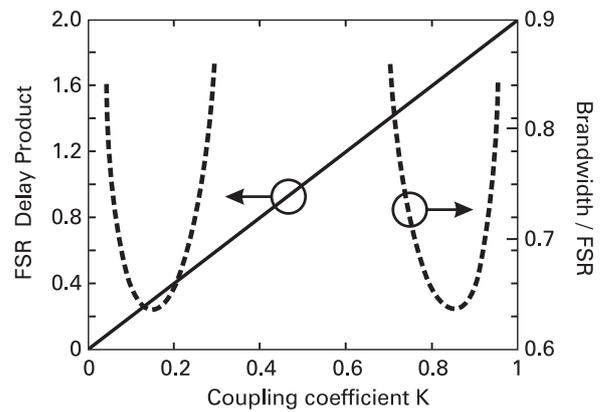


Figure 3 Characteristics of a two-stages Mach-Zehnder based tunable delay line

The photonic integrated delay line is perfectly suitable for the combination with other functionality, active devices as lasers, modulators and photodetectors and packaged in a single case with electrical or optical input and output. This solution, without moving parts is perfectly suitable for applications where speed, number of delays, reliability and costs are key factors.

For any solution shown in **Fig. 2**, the induced attenuation is proportional to the total time delay and



hence the choice of the most suitable technology (Silicon Photonics, Indium Phosphide or Silicon Nitride) is of key importance.

The Mach-Zehnder based delay line is patented¹ by Politecnico di Milano and it is available for exclusive and non-exclusive licensing.

Discuss your application with us

Each specific application requires a careful evaluation of the requested requirements in terms of maximum delay, delay resolution, attenuation, bandwidth, speed and control technique. A preliminary analysis permits to identify the most suitable technology.

Please contact the PICs4All consortium to know more about the use of PIC technology. The PICs4All is funded under the Horizon 2020 framework and brings together expertise to support end-users with PIC technology. We help you connecting to the ecosystem of designers, foundries, packaging and test services.

¹ Patent IT- 102017000053579

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Photonic Integrated Circuits for Quantum Technology

Quantum Technology (QT) is required for the application of quantum mechanics in a wide variety of fields. The EU Quantum Flagship¹ identifies four application areas, namely Quantum Computing, Quantum Simulation, Quantum Communication, and Quantum Sensing and Metrology. A variety of techniques and systems can be considered for such quantum-based technologies, including those based on cold ions, diamond vacancies, Josephson junctions, and photons. Besides such core technological choices, any real-world quantum system would also need enabling technologies, such as, for example, cryostats and ultra-low-noise electronics.

The opportunities of QT are wide-ranging and with a potentially huge impact. Quantum computers hold the promise of solving problems with unprecedented speed, or to tackle problems that current computers cannot even handle nowadays, i.e., the quantum advantage. Although such applications might still be over a decade away, other applications of QT have now been deployed and are getting close to commercialization, such as secure communication based on quantum key distribution.

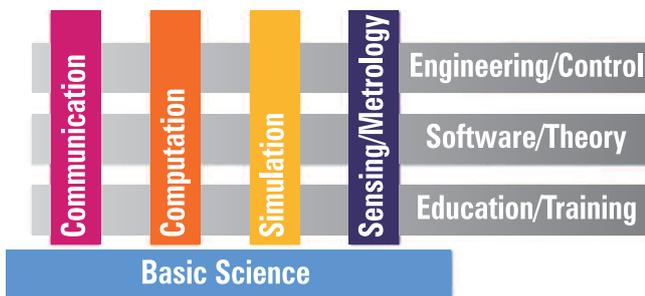


Figure 1 Strategic research agenda for the EU QT Flagship²

¹ <https://qt.eu/>

² <https://doi.org/10.1088/1367-2630/aad1ea>

The opportunity for photonic integration

Photonic integrated circuits (PICs) offer some very concrete opportunities for QT. In quantum communication, PICs are foreseen to be critical elements in the near-term deployment of metropolitan quantum-key-distribution-based secure systems². Individual and entangled photons can be generated, modulated and routed on the PIC. The existing use of PIC components and functionalities for wavelength-division multiplexed networks can be leveraged to enable practical quantum communication. Quantum entropy sources for gigabit-per-second random number generation are now being developed on a PIC by QuSide Technologies³.

In quantum computing, photons can be used for the encoding of qubits. PICs can be used for ultra-low loss, large-scale scalable linear optical circuits for routing, processing and analysis. The available nonlinearities can be utilized for photon pair generation. Based on such approaches, PsiQuantum is now building a general-purpose silicon photonic quantum computer⁴. QuiX has recently been founded to develop a single-purpose photonic quantum computer, based on silicon nitride PICs, for use in machine learning and quantum simulation applications⁵. Further integration of functionalities is possible, and, e.g., Xanadu is pursuing the integration of a squeezed light source on a PIC⁶.

Beyond quantum communication and photonic quantum computing, photonics, and hence PICs, can play an important role for other quantum technologies. Communication with and control of cryogenically cooled QT systems is better achieved through optical fiber access, for reasons of com-

³ <https://www.quside.com/>

⁴ <https://psiquantum.com/>

⁵ <https://nano-cops.com/news/cops-scientists-found-quantum-startup-quix>

⁶ <https://www.xanadu.ai/>

pactness and heat capacity⁷. Arguably, microwave photonics can replace conventional microwave technology for low-interference and compact systems. More explorative opportunities include the on-chip integration of ion traps and their optical addressing⁸.

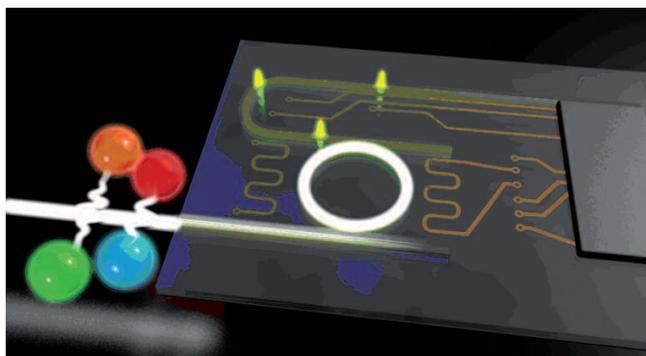


Figure 2 Artist impression of photon pair generation using a PIC, by Michael Kues, Aarhus University

Current technical developments

The PIC and overall system need to be carefully designed for the target application. Although the PIC technology platforms are mature, they have been developed mostly for telecom and datacom applications. QT might require a different design approach, based on a different trade-off. One critical difference is that many QT applications require ultra-low losses, with overall circuit insertion losses not exceeding the ~ 1 -dB level. On the other hand, high-speed operation well above 1 GHz is typically not required.

⁷ <http://www.scontel.ru/products/sspd/>

⁸ <http://dx.doi.org/10.1038/nnano.2016.139>

In the current mature PIC platforms, controlled single-photon emitters and single-photon detectors, like avalanche detectors (SPADs), are not available yet. Hybrid approaches can be pursued, whereby SPAD arrays are coupled to silicon nitride PICs, for example. Packaging facilities to enable such hybrid approaches are now commercially available, e.g., as offered by PHIX and LionIX⁹, and by the PIXAPP Photonic Packaging Pilot Line¹⁰.

Discuss your application with us

If you are interested to know more about the use of PIC technology for QT applications, please contact Martijn Heck, coordinator of the PICs4All Application Support Center (ASC) at Aarhus University, Denmark, or Michael Kues. We have experience with all major PIC platforms, i.e., silicon, silicon nitride and indium phosphide, for application in QT and related fields. Specific expertise includes nonlinear photonics, laser diodes, and high-speed and ultra-low loss PIC design. We are set up to help you to do a feasibility study for the use of PICs for QT applications.

The PICs4All consortium¹¹ is funded under the Horizon 2020 framework and brings together expertise to support end-users, like academia, research institutes and industry, with PIC technology. The ASCs can help you connect to the eco-system of designers, foundries, packaging and test services.

⁹ <https://photonics.lionix-international.com/packaging-service/>

¹⁰ <http://pixapp.eu/>

¹¹ <http://pics4all.jeppix.eu/>

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PIC Packaging and assembly

Interfacing Photonic Integrated Circuits with other components and to the outside world is realized via assembly and packaging processes. These include optical, electrical, thermal and mechanical processes put in place to interconnect a photonic IC with other components like electronic ICs, micro-optics, connectors to build a system on a chip (SoC) or system in a package (SiP) type of modules and interface those with operational environment.

An example of such co-package opto-electronics module based on CAD tool visualization is shown in **Fig. 1**. Many packaging and assembly solutions do exist, in particular for telecommunication applications. Those however, are typically proprietary, custom processes which are not readily accessible to external users. Moreover, the extent of customization in those processes resulted in absence of standard processes and tooling for assembly and packaging. At the same time maturity and accessibility¹ of the PIC fabrication technologies is leading to an increase in complexity of chips and wider range of possible applications for those. Consequently, the assembly and packaging can be a challenging and costly part of the integrated photonics production chain². Such impact can be reduced providing

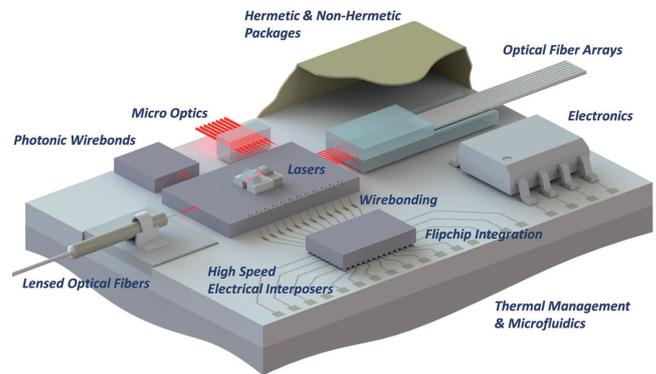


Figure 1 Example of co-packaged optoelectronic module from CAD tool (Image: www.pixapp.eu)

that packaging is put into consideration as early as possible in the manufacturing chain starting from idea and leading to a product as envisioned in **Fig. 2**. Design for packaging, reference templates and right paths through scalable processes will enable both efficient prototyping and ramp-up to volume production.

Prototype packaging via JePPIX

Along with multi-projects wafer runs (MPW) shuttles for PIC fabrication JePPIX consortium provides the PIC ecosystem with generic packaging solutions which further increase the accessibility and complements a rapid prototyping platform to PIC based products. Those services are available on a short

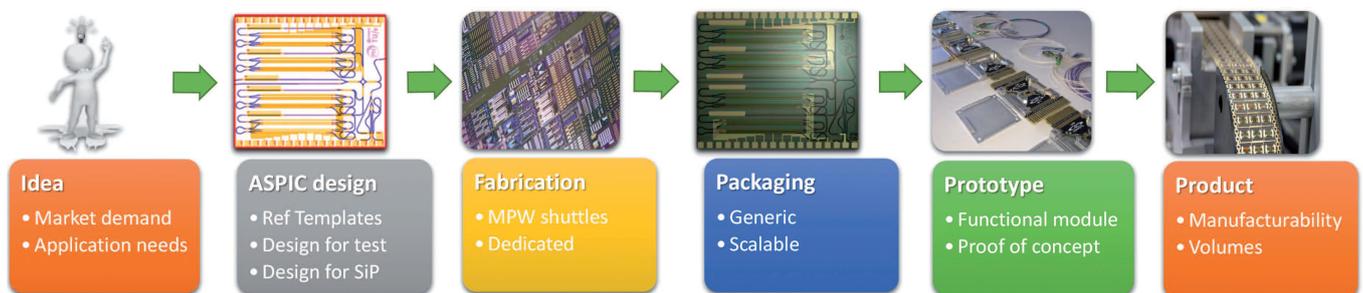


Figure 2 Manufacturing chain of application specific photonic integrated circuits product

¹ <http://www.jeppix.eu/multiprojectwafers>

² <http://www.jeppix.eu/vision>



turnover time providing that chips follow a reference layout taking into account assembly and packaging aspects outlined as design rules by the service suppliers³.

Pilot production via PIXAPP pilot line

In course of photonic integrated circuits assembly and packaging pilot line (PIXAPP) multiple front-end and back-end service providers collaborate on development of scalable assembly and packaging processes. Those processes enable a short path to ramp up to larger volume production. In addition to the process developments the PIXAPP offers intense, hands-on trainings in context of assembly and packaging of optoelectronics. Accessibility to the services offered is assured via single entry point via PIXAPP gateway⁴.

Access via PICs4All

Assembly and packaging aspects are important to be considered as early as possible in product development path. The PICs4All Application Support Centers (ASCs)⁵ will guide you through whether it is the first experience with photonic integration technologies and requires a rapid prototyping path or if your concept has already been proven for application with a successful prototype and requires a scale up scenario for production.

³ <http://www.jeppix.eu/packaging>

⁴ <https://pixapp.eu>

⁵ <http://pics4all.jeppix.eu/get-support.html>

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About PICs4All

PICs4All (Photonic Integrated Circuits Accessible to Everyone) is a Coordination and Support Action from the EU H2020 ICT-27-2015 programme. The prime objective of PICs4All is to increase the impact of photonics and enable an access to the advanced photonic integrated circuit (PIC) technologies for academia, research institutes, SMEs and larger companies. This will be achieved by establishing a European network of Application Support Centres (ASCs) in the field of PIC technology. The main task of the ASCs is to lower the barrier to researchers and SMEs for applying advanced PICs, and thus to increase the awareness of the existence of the worldwide unique facility provided by JePPiX (InP and TriPLeX PIC design, manufacturing, testing and packaging).

The main PICs4All objectives:

- scouting, acquiring and supporting new PIC users;
- promoting the use of the European photonic integration platforms;
- strengthening Europe's industrial lead in the business of integrated photonics;
- bringing together academia to explore photonics and promote its critical importance.

The PICs4All consortium:

- actively explores the market, searching for new application fields for ASPICs;
- offers guided access to Multi-Project Wafer runs for ASPIC fabrication;
- provides support in ASPIC design and prototype testing;
- connects users to professional design houses and packaging vendors;
- organizes ASPIC design courses and workshops.

PICs4All ASCs will actively support users in taking full advantage of the PIC-technology and its deployment in existing and new applications. For this reason, it combines two targets of an EC supported

CSA, i.e. enabling the access to advanced design, fabrication and characterisation facilities, and stimulating the innovation potential of users, esp. SMEs, by supplying hands-on support in developing their business cases. All this is achieved by connecting existing PIC-development infrastructure throughout Europe and by lowering the risk at the investment stage in PIC development by enabling access to low-cost prototyping.

Fact and Figures:

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Project acronym:	PICs4All (Photonic Integrated Circuits Accessible to Everyone)
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Budget:	1 051 895,- EUR
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Partners:

The PICs4All consortium consists of nine academic research institutes with a good regional balance throughout Europe, enabling Application Support Centres in Germany, United Kingdom, France, Denmark, Spain, Poland, Italy, Greece, the Netherlands. It also includes the EPIC association located in France and Berenschot in the Netherlands.

Members of the consortium:

Eindhoven University of Technology
University of Cambridge
Universitat Politècnica de València
Politecnico di Milano
Warsaw University of Technology
Technische Universität Berlin
Aarhus University
Telecom ParisTech
National Technical University of Athens
European Photonics Industry Consortium
Berenschot